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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 06/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,023	PEREGO ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-107* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-107* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communication filed on April 14, 2006. This amendment has been entered and carefully considered. Claims 1, 21, 60 and 101-107 are amended and claims 1-107 are presented again for examination.

2. Applicant's arguments filed on April 14, 2006 have been fully considered but they are not deemed to be persuasive.

3. The rejection of claims 1-107 as in the previous Office Action is respectfully maintained and reiterated below for Applicant's convenience.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-23, 28, 30-44, 46-47, 52, 62-68, 76-84, 86, 92-93, 98, 100-103 and 105-106 are rejected under 35 U.S.C. 102(e) as being anticipated by Roohparvar (USPN: 2005/0259506).

As per claim 1, Roohparvar teaches a method for scheduling a device command comprising issuing a first device command (i.e. the READ command); and issuing a first

value (i.e. m clocks) associated with the first device command, wherein the first value determines, at least in part, a first performance time at which the first device command is to be performed (e.g. see paragraph [0077] and Fig. 3).

As per claim 2, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the step of issuing a first device command comprises: issuing a first memory device command and the first performance time is a time at which the first memory device command is to be performed (i.e. at n+m clock edge) (e.g. see paragraph [0077]).

As per claim 3, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the step of issuing a first memory device command occurs at a first issuance time (i.e. at T0 in Fig. 3) and the step of issuing a first value occurs at a second issuance time (i.e. at T2 in Fig. 3) (e.g. see paragraph [0077] and Fig. 3).

As per claim 4, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first issuance time and the second issuance time are different (i.e. To and T2 are different) (e.g. see Fig. 3).

As per claims 5 and 19, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the difference between the first issuance time and the second issuance time is a time gap (i.e. the time gap of T2 – T0) (e.g. see Fig. 3).

As per claims 6 and 20, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the time gap is predetermined, i.e. the latency can be set to one, two or three clock cycles (e.g. see paragraph [0077]).

As per claim 7, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the time gap is fixed, i.e. the latency can be set to a fix value such as one, two or three clock cycles (e.g. see paragraph [0077]).

As per claims 8, 103 and 106, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first value is a first delay value (i.e. m clocks) (e.g. see paragraph [0077]).

As per claims 9 and 10, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first delay value (i.e. m clocks) is expressed relative to a standardized unit of time and it is expressed in units of a clock period (i.e. the clock cycles) (e.g. see paragraph [0077]).

As per claim 11, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first delay value denotes an integer multiple of a clock period, i.e. one, two or three clock cycles (e.g. see paragraph [0077]).

As per claim 12, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first delay value denotes a submultiple of a clock period, i.e. one, two or three clock cycles (e.g. see paragraph [0077]).

As per claims 13 and 76, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first delay value has a positive, i.e. one, two or three clock cycles (e.g. see paragraph [0077]).

As per claim 14, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first delay value has a value greater than zero, i.e. one, two or three clock cycles (e.g. see paragraph [0077]).

As per claims 15, 77 and 78, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that a delay between the first issuance time and the first performance time is determined by the first delay value (i.e. T1-T0 in Fig. 3 with CAS latency = 2) and an additional delay value (i.e. T2-T1 in Fig. 3 with CAS latency = 2) (e.g. see Fig. 3 and paragraph [0077]).

As per claim 16, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that a delay between the first issuance time (i.e. at TO in Fig. 3) and a first decoding time (i.e. at T2 in Fig. 3) at which the first memory device command is decoded is determined by the first delay value (i.e. T1-T0 in Fig. 3 with CAS latency = 2) and an additional delay value (i.e. T2-T1 in Fig. 3 with CAS latency = 2) (e.g. see Fig. 3 and paragraph [0077]).

As per claim 17, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that a delay between a first decoding time at which the first memory device command is decoded and the first performance time is determined by the first delay value (i.e. T1-T0 in Fig. 3 with CAS latency = 2) and an additional delay value (i.e. T2-T1 in Fig. 3 with CAS latency = 2) (e.g. see Fig. 3 and paragraph [0077]).

As per claim 18, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first issuance time and the second

issuance time are the same if the latency, i.e. the delay (m) value is set same for both first and second READ commands (e.g. see paragraph [0077]).

As per claim 21, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first memory device command is a column access strobe (CAS) command (e.g. see paragraph [0077]).

As per claim 22, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the time gap is known at or before the first issuance time i.e. one, two or three clock cycles (e.g. see paragraph [0077]).

As per claims 23, 47 and 93, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first memory device command is a precharge command (e.g. see paragraph [0088]).

As per claims 28, 52 and 98, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first memory device command is a mode register operation command (e.g. see paragraph [0057] and Fig. 24).

As per claims 30-31 and 46, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that a first parameter, i.e. the memory address, associated with the first memory device command (i.e. the READ command) is queued until the first performance time (i.e. the memory address will be queued in the READ command until the READ command get executed) (e.g. see paragraph [0077]).

As per claim 32, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first value is communicated from a memory controller (i.e. 340 in Fig. 32) to a first memory device (i.e. 350 in Fig. 32) (e.g. see Fig. 32).

As per claims 33 and 102, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first value (i.e. m clock cycles) is communicated from the first device, i.e. a memory controller (i.e. 340 in Fig. 32) to the second device, i.e. a first memory device (i.e. 350 in Fig. 32) (e.g. see Fig. 32).

As per claim 34, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches about issuing a second device command (i.e. the second/another READ command); and issuing a second value (i.e. m clocks), wherein the second value determines, at least in part, a second performance time at which the second device command is to be performed (e.g. see paragraph [0077] and Fig. 3).

As per claims 35, 81 and 88, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the step of issuing a first device command comprises issuing a first memory device command, the step of issuing a second device command comprises issuing a second memory device command, the first performance time is a first time at which the first memory device command is to be performed (i.e. at n+m clock edge), and the second performance time is a second time at which the second memory device command is to be performed (i.e. at additional n+m clocks edge) (e.g. see paragraph [0077]).

As per claims 36 and 82, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the step of issuing the first memory device command (i.e. the (first) READ command) occurs at a first issuance time, the step of issuing the first value (i.e. m clocks) occurs at a second issuance time, the step of issuing the second memory device command (i.e. the (next/second) READ command) occurs at a third issuance time, and the step of issuing the second value (i.e. the additional m clocks) occurs at a forth issuance time (e.g. see paragraph [0077]).

As per claims 37-39 and 63, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first issuance time is the same as the second issuance time, i.e. the (first) READ command is registered at clock edge n and at the same time the latency of m clocks is registered; and the third issuance time is the same as the fourth issuance time, i.e. the (second/next) READ command is registered at clock edge n and at the same time the latency of (additional) m clocks is registered (e.g. see paragraph [0077]). Since the next/additional READ command get issued after the first READ command is issued and processed, the first issuance time (i.e. for the first READ command) and the third issuance time (i.e. for the next/additional READ command) are different. And since the first issuance time is the same as the second issuance time and the third issuance time is the same as the fourth issuance time, a first difference between the first issuance time and the second issuance time is of equal duration to a second difference between the third issuance time and the fourth issuance time.

As per claim 40, Roohparvar teaches the claimed invention as described above and furthermore, as described above in rejection of claim 37, Roohparvar teaches that the (first) READ command is registered at clock edge n and at the same time the latency of m clocks is registered, the first difference is known at the first issuance time (e.g. see paragraph [0077] and Fig. 3).

As per claims 41, 62, 84 and 86, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first value is a first delay value (i.e. the m clocks) and the second value is a second delay value (i.e. the additional m clocks) (e.g. see Fig. 3).

As per claims 42 and 83, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the second delay value (i.e. the additional m clocks) is the same as the first delay value (i.e. the m clocks), i.e. even if the first READ command and additional/next READ command are issued at different times, the delay time is still same and equal to m clocks (e.g. see Fig. 3), however, since the latency, i.e. the delay (m) value can be set to either one, two or three clock cycles, if the m value is set different at the first READ command time than at the second READ command time, then the second delay value will different than the first delay value as claimed (e.g. see paragraph [0077]).

As per claim 43, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the second delay value (i.e. the additional m clocks) is the same as the first delay value (i.e. the m clocks), i.e. even if the first READ

command and additional/next READ command are issued at different times, the delay time is still same and equal to m clocks (e.g. see Fig. 3).

As per claims 44 and 100, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first performance time is after the second performance time, i.e. the execution of (first) READ command is after the execution of (next/additional) READ command when the value of m is two or three clocks in (first) READ command and the value of m is one clock in (next/additional) READ command (e.g. see paragraph [0077]).

As per claim 64, Roohparvar teaches a controller (i.e. 340 in Fig. 32) for scheduling commands comprising a driver for issuing commands and associated non-zero delay values to at least one device (i.e. 350 in Fig. 32) coupled to the controller, wherein a first delay value (i.e. m clocks) is associated with a first performance time at which a first command (i.e. the READ command) of the commands is to be performed by the device (e.g. see paragraph [0077] and Figs. 3 and 32).

As per claim 65, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the driver comprises a first driver for issuing commands (i.e. READ command) to the device and a second driver for issuing delay values (i.e. m clocks delay) to the device (i.e. DRAM 350 in Fig. 32) (e.g. see paragraph [0077] and Figs. 3 and 32).

As per claims 66 and 92, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the controller is a memory controller (i.e. 340 in Fig. 32).

As per claim 67, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the device is a memory device (i.e. 350 in Fig. 32).

As per claim 68, see argument with respect to the rejection of claims 2 and 35. Claim 68 is also rejected based on the same rationale as the rejection of claims 2 and 35.

As per claim 79, Roohparvar teaches a device comprising a receiver (i.e. the command register in Fig. 1A) for receiving a first device command, a first value (i.e. the m clocks) associated with the first device command (i.e. the READ command), wherein a first performance time is associated with the first value; means for performing the first device command at the first performance time; and control circuitry for controlling the means to cause the means to perform the first device command at the first performance time (e.g. see Figs. 1A and 3 and paragraph [0077]).

As per claim 80, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the receiver is also for receiving a second device command (i.e. the next/second READ command) and a second value (i.e. additional m clocks) associated with the second device command (e.g. see paragraph [0077]).

As per claims 101 and 105, Roohparvar teaches a system comprising a first device (i.e. the command register in Fig. 1A) configured to issue commands (i.e. READ commands) and values (i.e. delay values), wherein each of the values is associated with a respective one of the commands; and a second device (i.e. the command register

in Fig. 1A) configured to receive the commands (i.e. READ commands) and the associated values (i.e. delay values); the second device further configured to execute each command at a time determined at least in part by the value associated with the command, wherein the first device is further configured to dynamically determine the value associated with at least one of the commands (e.g. see paragraph [0077] and Figs. 1A and 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 24-27, 29, 48-51, 53, 59-60, 69-75, 94-97 and 99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roohparvar.

As per claims 24-27, 29, 48-51, 53, 94-97 and 99, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first memory device command is a READ command, a precharge command or a mode register command as described above in rejection of claims 1, 23 and 28, respectively. As admitted by the Applicant that the first memory device command may be, for example, a CAS command, a precharge command, a RAS command, a refresh command, a command including the functionality of refresh and the RAS commands, a command including the functionality of refresh and the precharge commands, a mode

register operation command, a power mode command, or another command (e.g. see paragraph [0035] of this application). Therefore, as admitted by the Applicant, not only READ, precharge or mode register commands, but any command can be used as the first memory device command. Based on this rationale, claims 24-27, 29, 48-51, 53, 94-97 and 99 are rejected.

As per claims 69-75, Roohparvar teaches the claimed invention as described above and furthermore, Roohparvar teaches that the controller determines the first and second performance times (i.e. the first and second delay values). The further limitations that the performance constrains are dependent upon (i) a physical location relative to the controller, (ii) a propagation delay affecting the reception of the first command and the data, (iii) a state of the device, (iv) the operation speed limitation of the device and (v) the timing granularity difference between an internal bus and an external bus of the device, are well-known and notorious old in the art at the time of current invention was made. It is well-known and notorious old in the art that by increasing the distance between the device physically located from the controller, the propagation delay increases which reduces the performance.

As per claims 59 and 60, Roohparvar teaches the claimed invention as described above and furthermore, the first and second address (i.e. the first READ address and the second READ address) may or may not be same address because it depends on the first and second READ commands, i.e. if the first and second READ commands are for the same addresses, then first and second addresses are same otherwise not (e.g. see Fig. 3 and paragraph [0077]).

6. Claims 45, 54-58, 61, 85, 87-91, 104 and 107 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roohparvar in view of Cashion et al. (USPN: 6,195,434) hereinafter, Cashion.

As per claim 55, Roohparvar teaches the claimed invention as described above but failed to teach about having a look-up table. Cashion, on the other hand, teaches a look-up table (i.e. the table shown in Fig. 3) having a plurality of delay values (i.e. range delay values shown in forth column) and associated addresses (i.e. the range index shown in first column), wherein each of the delay values is associated with one of the addresses, wherein the first index value represents one of the addresses in the look-up table, and wherein the step of determining the first delay value comprises selecting the delay value associated with the address of the first index (e.g. see Fig. 3 and Col. 3, lines 39-56).

As per claims 45, 54, 56, 85, 87-88, 104 and 107, the combination of Roohparvar and Cashion teaches the claimed invention as described above and furthermore, Cashion teaches that the first value is a first index value (i.e. 0 in first column of Fig. 3) and the second value is a second index value (i.e. 1-20 in first column of Fig. 3) (e.g. see Fig. 3).

As per claim 57, the combination of Roohparvar and Cashion teaches the claimed invention as described above and furthermore, Cashion teaches that the delay values are determined based on the corresponding index values associated with it as shown in Fig. 3 table, i.e. the first delay value is determined based on the first index

value and the second delay value is determined based on the second index value (e.g. see Fig. 3).

As per claim 58, see arguments with respect to the rejection of claims 55 and 57. Claim 58 is also rejected based on the same rationale as the rejection of claims 55 and 57.

As per claim 61, the combination of Roohparvar and Cashion teaches the claimed invention as described above and furthermore, Cashion teaches that the step of providing a look-up table comprises the steps of providing a first look-up table and a second look-up table, and wherein the first address is associated with the first look-up table (i.e. the look-up table comprising first row in Fig. 3) and the second address is associated with the second look-up table (i.e. the look-up table comprising second row in Fig. 3).

As per claims 89-91, the combination of Roohparvar and Cashion teaches the claimed invention as described above and furthermore, Roohparvar teaches that the first and second receivers (i.e. the command registers in Fig. 1A) are configured to receive the first and second device commands (i.e. READ commands) and the first and second indices from a controller (i.e. 340 in Fig. 32).

Remarks

7. As to the remark, Applicant asserted that:

(a) Roohparvar does not teach, or even suggest, that "m clock" bits are associated with a specific command (e.g., a first device command). In

contrast, the "m clock" bits as disclosed by Roohparvar represent the CAS latency delay for all READ commands. Thus, Roohparvar does not teach, or even suggest, issuing a first value associated with the first device command, as presently claimed.

(b) Roohparvar does not teach, or even suggest, that these "m clock" bits are issued associated with the READ command. Indeed, Roohparvar does not teach, or even suggest, that these "m clock" bits are issued in any manner. Thus, Roohparvar does not teach, or even suggest, issuing a first value associated with the first device command, as presently claimed.

(c) Roohparvar does not teach, or even suggest, that these "m clock" bits determine, at least in part, a time at which the READ command is performed. In contrast, the "m clock" bits as disclosed by Roohparvar merely represent the CAS latency delay between the registration of a READ command and the availability of read data on output lines of a memory device. Indeed, the READ command as disclosed by Roohparvar is performed as soon as it is registered. That is, it is only the availability of read data on output lines of the memory device that is delayed by the latency represented by the "m clock" bits, not the performance of the READ command. Thus, Roohparvar does not teach, or even suggest, issuing a first value associated with the first device command, wherein the first value determines, at least in part, a first performance time at which the first device command is to be performed, as presently claimed.

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a), Roohparvar does clearly teach that "m clock" bits are associated with a specific command (i.e. **a** READ command). Roohparvar discloses in lines 5-7 of paragraph [0077] on page 5, "For example, if a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge n+m", in other words, the m clocks latency is associated with the READ command.

With respect to (b), Roohparvar discloses in lines 4-5 of paragraph [0077] on page 5, "The latency can be set to one, two or three clocks cycles.", in other words, the latency of m clock bits is issued/set for the READ command(s) as claimed.

With respect to (c), since the data requested by the READ command is not available until the clock edge n+m, the READ command cannot be called fully performed until the data is available, i.e. until the clock edge n+m. Therefore, the Roohparvar prior art still reads on the claimed limitation.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HBP
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SUPERVISORY PATENT EXAMINER
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